What is claimed is:

1. A nonvolatile memory comprising a memory array including a plurality of nonvolatile memory cells permitting electrical writing and erasing of information to be stored and storing information correspondingly to a threshold voltage, said nonvolatile memory performing writing and erasing in prescribed units, comprising:

a replacing function to replace a group of memory cells including defective memory cells which are incapable of normal writing or erasing with a group of memory cells including no defective memory cell;

a numbers of rewrites averaging function to grasp the number of data rewrites in each group of memory cells and to perform replacement of memory cell groups such that there may arise no substantial difference in the number of rewrites among a plurality of memory cell groups; and

an error correcting function to detect and correct any error in data stored in said memory array,

wherein first address translation information deriving from said replacing function and second address translation information deriving from said numbers of rewrites averaging function are stored in respectively prescribed areas in said memory array, and

wherein said first address translation information and second address translation information concerning the same memory

cell group are stored in a plurality of sets in a time series.

2. The nonvolatile memory according to Claim 1, wherein the plural sets of first address translation information and second address translation information are stored in some of a plurality of first areas into which writing is done separately.

3. The nonvolatile memory according to Claim 2, wherein said memory array includes two or more second areas which are different areas from said first areas, and said plural sets of first address translation information and second address translation information are stored in said first areas and said second areas alternately.

4. The nonvolatile memory according to Claim 3, wherein information indicating the orders of said first address translation information and second address translation information in the time series is stored in said first areas where the respectively corresponding address translation information are to be stored.

5. The nonvolatile memory according to Claim 4, wherein said time series information is referenced at the time of turning on power supply and said replacement and averaging of the numbers of rewrites are executed by using the latest address translation information in time series.

6. The nonvolatile memory according to Claim 5, further including a memory circuit comprised of volatile memory cells,

wherein said latest address translation information in time

series is read out to said memory circuit at the time of turning on power supply, and said replacement and averaging of the numbers of rewrites are executed by using the address translation information held in the memory circuit.

7. The nonvolatile memory according to Claim 6, wherein the address translation information held in said memory circuit is written into said memory array when power supply is interrupted.

8. The nonvolatile memory according to Claim 7, wherein said averaging of the numbers of rewrites is so configured that, said memory array is divided into a plurality of blocks, and when the number of writes in a memory cell group in any block has reached a prescribed number, rotation of an object of writing is performed in another block among memory cell groups of which the offset values from the leading position in the block are the same.

9. The nonvolatile memory according to Claim 8, wherein a plurality of memory cell groups connected to the same word line is made the unit of writing, a first buffer memory and a second buffer memory are provided each having a storage capacity at least greater than the unit of writing and capable of holding data read out from said memory array, and parallel reading is made possible by alternately using these buffer memories.

10. The nonvolatile memory according to Claim 9,

wherein at the time of writing data into said memory array,

after causing said first buffer memory or second buffer memory to hold rewrite data inputted from outside and causing said

second buffer memory or first buffer memory to hold data read out from the memory cell group which is the write object,

the memory cell group which is the write destination is varied into an erased state, the rewrite data held in said first buffer memory or second buffer memory are written into the corresponding position in said second buffer memory or first buffer memory, and

wherein the data held in second buffer memory or first buffer memory are caused to be stored in the memory cell group which is the write object.

11. The nonvolatile memory according to Claim 10,

wherein when management data and other data than the management data are to be stored in said memory cell group,

at the time of erasing data in said memory array, data corresponding to the erased state of the memory cell on all the bits in said first buffer memory or second buffer memory is set, and then, data which are read out from the memory cell group and are to be erased, are caused to be held in said second buffer memory or first buffer memory, thereafter,

the memory cell group which is the write object is varied into the erased state, and the data corresponding to the erased state held in said first buffer memory or second buffer memory are written into the corresponding position in said second buffer memory or first buffer memory, and

the data held in second buffer memory or first buffer memory

are caused to be stored in the memory cell group of an erasing object.

12. The nonvolatile memory according to Claim 11, wherein, when power supply is turned on in a state in which a prescribed signal is entered from outside, data in a prescribed area in said memory array can be read out and supplied from a prescribed terminal.

13. The nonvolatile memory according to Claim 12, wherein, when a prescribed signal is entered from outside in a state in which power supply is on, data in a prescribed area in said memory array can be read out and supplied from a prescribed terminal.

14. The nonvolatile memory according to Claim 13, further including an internal power supply circuit for generating a voltage required for writing into said memory array and erasing data,

wherein the operation of said internal power supply circuit can be stopped in accordance with the inputting of a prescribed command code from outside.